ORIGINAL PROVISIONAL

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APPL NO.	FILING OR 371 (c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
60/460,495	04/03/2003		160	59305-8085.US00	9		

CONFIRMATION NO. 9822

CORRECTED FILING RECEIPT

OC000000010597138

22918
PERKINS COIE LLP
P.O. BOX 2168
MENLO PARK, CA 94026

Date Mailed: 07/30/2003

Receipt is acknowledged of this provisional Patent Application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Matthew Waight, Pipersville, PA;
James Marsh, Sherwood, OR;
Howard Luong, Hong Kong, CHINA;

If Required, Foreign Filing License Granted: 06/09/2003

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

Electronically tuned agile integrated bandpass filter

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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Resp.Office: MEN

Case Number: 593058085
Country: US
SubCase:
Client: Maxim Integrated Products
United States of America
Case Type: PRO
Application Status: Pending
Application Number: 60/460,495
Filing Date: 03-Apr-2003
Publication Number:
Publication Date:
Patent Number:
Issue Date:
Parent/PCT Number:
Parent/PCT Date :
Parent Patent Number:
Parent Issue Date :
Tax Schedule: LE
Expiration Date:
Confirmation Number:
Patent Term Adjustment: 0
Agent:
Agent Reference No.:

PC Client Ref. Number: SN-MAXM-301
Appeal Number:
Client Remarks:

List Of Actions

Action(s) Due	Due Date		Action Taken
Postcard Received?	03-May-2003	Due Date	23-May-2003
Filing Receipt Received?	03-Jul-2003	Due Date	01-Aug-2003
Missing Parts Received?	03-Jul-2003	Due Date	03-Apr-2003
Req. Corrected Filing Reciept	10-Jul-2003	Due Date	08-Jul-2003
Await. Req. Corr. Filing PC	08-Aug-2003	Due Date	21-Jul-2003
Await. Corrected Filing Rec.	08-Oct-2003	Due Date	01-Aug-2003
File NonProvisional (3-mo adv)	03-Jan-2004	Reminder	
Foreign Filing (3-mo adv)	03-Jan-2004	Reminder	
File NonProvisional (1-mo adv)	03-Mar-2004	Reminder	
Foreign Filing (1-mo adv)	03-Mar-2004	Reminder	
File NonProvisional	03-Apr-2004	Final	
Foreign Filing	03-Apr-2004	Final	

User ID: Hung

Date Created: 07-Feb-2003

Last Update: 09-Jul-2003

Shary

Country Application

Wednesday, July 09, 2003 Page: 1

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Publication Date:
Patent Number:
Issue Date:
Parent/PCT Number:
Parent/PCT Date :
Parent Patent Number:
Parent Issue Date :
Tax Schedule: LE
Expiration Date:
Confirmation Number:
Patent Term Adjustment: 0
Agent:
Agent Reference No.:

PC Client Ref. Number: SN-MAXM-301
Appeal Number:
Client Remarks:

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Foreign Filing (1-mo adv)	03-Mar-2004	Reminder	
File NonProvisional	03-Apr-2004	Final	
Foreign Filing	03-Apr-2004	Final	

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Date Created: 07-Feb-2003

Last Update: 09-Jul-2003

IN RE APPLICATION OF:

WAIGHT ET AL.

APPLICATION NO.: 60/460,495

FILED: APRIL 3, 2003

FOR: ELECTRONICALLY TUNED AGILE INTEGRATED BANDPASS FILTER

ATTORNEY DOCKET NO.:

59305-8085.US00

DATE OF THIS MAILING:

JULY 8, 2003

RECEIVED BY THE U.S. PATENT and Trademark Office:

Papers Enclosed

1. Request for Corrected Filing Receipt
2. Copy of Filing Receipt and red-lined copy of filing receipt
3. Copies of originally filed Utility patent application transmittal, return post card and express mail receipt
4. Postcard receipt.

CMT/srb

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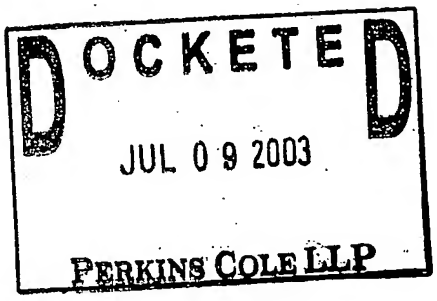

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on:

Date: July 8, 2003 By: Sharyl Brown
Sharyl Brown

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Waight *et al.*	EXAMINER: Unknown
APPLICATION NO.: 60/460,495	CONFIRMATION NO.: 9822
FILED: April 3, 2003	
FOR: ELECTRONICALLY TUNED AGILE INTEGRATED BANDPASS FILTER	

Request for Corrected Filing Receipt

Commissioner for Patents
PO Box 1450
Alexandria, D.C. 22313-1450

Sir:

1. Attached is a copy of an official filing receipt received from the U.S. Patent and Trademark Office for which a corrected filing receipt is respectfully requested.

2. There is an error in the filing date, which was incorrectly entered. The filing date should read –April 3, 2003--. Enclosed is a redlined copy of the Filing Receipt showing the requested change, along with copies of the originally filed Transmittal of Utility Patent Application, Return postcard and Express Mail Receipt all evidencing the filing date of April 3, 2003.

3. Applicants believe that the correction is not due to any Applicant's error, therefore no fees are necessary. However, if the Commissioner deems that Applicant's errored, then the Commissioner is authorized to obtain the appropriate fee from deposit account no. 50-2207.

Respectfully submitted,
Perkins Coie LLP

Date: July 8, 2003

Carin M. Tan
Registration No. 45,769

Correspondence Address:
Customer No. 22918
Perkins Coie LLP
P.O. Box 2168
Menlo Park, California 94026
(650) 838-4300

BRC

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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60/460,495	04/04/2003		160	59305-8085.US00	9		

22918
PERKINS COIE LLP
P.O. BOX 2168
MENLO PARK, CA 94026

CONFIRMATION NO. 9822

FILING RECEIPT

OC000000010222795

Date Mailed: 06/10/2003

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Early Publication Request: No

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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
60/460,495	~~04/04/2003~~ 04/03/2003		160	59305-8085.US00	9		

CONFIRMATION NO. 9822

22918
PERKINS COIE LLP
P.O. BOX 2168
MENLO PARK, CA 94026

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JUN 17 2003
PERKINS COIE LLP

FILING RECEIPT

OC000000010222795

Date Mailed: 06/10/2003

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Waight, *et al.*	EXAMINER: Unassigned
APPLICATION NO.: Unassigned	ART UNIT: Unassigned
FILED: Concurrently Herewith	
FOR: **ELECTRONICALLY TUNED AGILE INTEGRATED BANDPASS FILTER**	

Request for Filing a Provisional Patent Application Under 37 CFR §1.53(c)

Box Provisional Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This is a request for filing a Provisional Application for Patent under 37 CFR §1.53(c).

1. **Title of Invention:**

ELECTRONICALLY TUNED AGILE INTEGRATED BANDPASS FILTER

2. **Inventor Applicant(s):**

Last Name	First Name	Residence (City and either State or Foreign Country)
Waight	Matthew	Pipersville, Pennsylvania
Marsh	James	Sherwood, Oregon
Luong	Howard	Hong Kong, China

3. **Correspondence Address:**

Customer No. 22918
Perkins Coie LLP
P.O. Box 2168
Menlo Park, California 94026
(650) 838-4300

4. **Enclosed documents accompanying this transmittal sheet:**

- ☒ Return Post card for USPTO Date Stamp
- ☒ Specification Number of pages: 19
- ☒ Certificate of Express Mail
- ☒ Other: Cover Sheet

☒ Claims Number of pages: 06 ☐ Other: _____

☒ Abstract Number of pages: 01 ☐ Other: _____

☒ Drawings Number of pages: 09 ☐ Other: _____

5. **Government Interest**

☐ This invention was made by an agency of the United States Government, or under contract with an agency of the United States Government. The name of the U.S. Government Agency and the Government contract number are:

6. **Method of Payment**

☐ Applicant claims small entity status. See 37 CFR §1.27.

☒ Please charge the Filing Fee $160) and any other fees necessary for timely filing of this application to Deposit Account No. 50-2207.

Respectfully submitted,

Date: April 3, 2003

Glenn E. Von Tersch
Registration No. 41,364

Correspondence Address:
Customer No. 22918
(650) 838-4300

PROVISIONAL APPLICATION FILING ONLY

GVT

Attorney Docket No.:	Date Mailed:	Express Mail No.
59305-8085.US00	April 3, 2003	EV 057 403 007 US

Applicant: Waight, et al.

Title: ELECTRONICALLY TUNED AGILE INTEGRATED BANDPASS FILTER

Papers Enclosed

- ☒ Transmittal Letter
- ☒ SPECIFICATION — 19 pages
- ☒ Claims — 06 page
- ☒ Abstract — 01 page
- ☒ Drawings — 09 sheets
- ☒ Check

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60/460492
04/03/03

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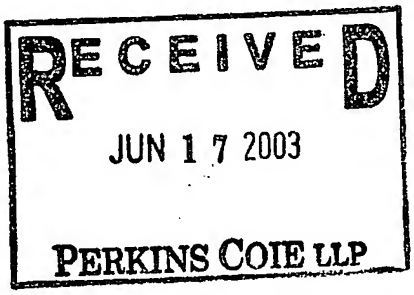

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59305-8085.US00	April 3, 2003	EV 057 403 007 US

Applicant: Waight, et al.

Title: ELECTRONICALLY TUNED AGILE INTEGRATED BANDPASS FILTER

Papers Enclosed

- ☒ Transmittal Letter
- ☒ SPECIFICATION 19 pages
- ☒ Claims 06 page
- ☒ Abstract 01 page
- ☒ Drawings 09 sheets
- ☒ Check

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IN RE APPLICATION OF: Waight, *et al.*	EXAMINER: Unassigned
APPLICATION NO.: Unassigned	ART UNIT: Unassigned
FILED: Concurrently Herewith	
FOR: **ELECTRONICALLY TUNED AGILE INTEGRATED BANDPASS FILTER**	

Request for Filing a Provisional Patent Application Under 37 CFR §1.53(c)

Box Provisional Patent Application
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Sir:

This is a request for filing a Provisional Application for Patent under 37 CFR §1.53(c).

1. **Title of Invention:**

ELECTRONICALLY TUNED AGILE INTEGRATED BANDPASS FILTER

2. **Inventor Applicant(s):**

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4. **Enclosed documents accompanying this transmittal sheet:**

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5. **Government Interest**

☐ This invention was made by an agency of the United States Government, or under contract with an agency of the United States Government. The name of the U.S. Government Agency and the Government contract number are:

6. **Method of Payment**

☐ Applicant claims small entity status. See 37 CFR §1.27.

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Respectfully submitted,

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UNITED STATES PROVISIONAL PATENT APPLICATION

FOR

ELECTRONICALLY TUNED AGILE INTEGRATED BANDPASS FILTER

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ELECTRONICALLY TUNED AGILE INTEGRATED BANDPASS FILTER

FIELD

[0001] The present invention relates to the field of communications systems. More particularly, the present invention relates to electronic circuitry for use as a tuner in a communications system.

BACKGROUND

[0002] Increasing use of wireless and high frequency technology in consumer products has resulted in more radiated signals in portions of the spectrum available for such products. Noise of various kinds can be injected into integrated circuits, thus reducing performance. One instance of such noise is beats – interference between two oscillators operating at similar frequencies. Another instance of such noise is harmonics – energy at a frequency related to an oscillator frequency produced due to non-ideal (real-world) aspects of circuit components. Both of these instances of noise are preferably reduced in circuits.

[0003] Preferably, blocking or reducing noise injected into circuits and systems is achieved in an inexpensive manner. Noise may be injected due to adjacent channels, image tones, jamming or blocking signals, and for other reasons. However, blocking or reducing noise is not the primary function of a system, it is a necessary addition allowing the rest of the system to perform its intended function, such as receiving encoded television or audio signals for example.

[0004] Shown in Figure 1A is a block diagram illustrating the mixing or converting of a bandpass signal by a periodic signal. As shown, a bandpass signal, $x(t) = f(t)\cos(\omega_1 t)$, is provided at input 102. The function, $f(t)$, has Fourier transform, $F(s)$, such that the bandpass signal, $x(t)$, has Fourier transform, $X(s)$. Moreover, using known characteristics of the Fourier transform, the Fourier transform, $X(s)$, of the bandpass signal, $x(t)$, can be written as

$$X(s) = F(s) * \mathrm{II}(s) = F(s) * \frac{\pi}{\omega_1}\left(\tfrac{1}{2}\delta\left(\frac{\pi}{\omega_1}s + \tfrac{1}{2}\right) + \tfrac{1}{2}\delta\left(\frac{\pi}{\omega_1}s - 1\tfrac{1}{2}\right)\right)$$

[0005] which after some manipulation becomes

$$X(s) = \tfrac{1}{2}F(s + \frac{\omega_1}{2\pi}) + \tfrac{1}{2}F(s - \frac{\omega_1}{2\pi}).$$

[0006] As further shown in Figure 1A, a periodic signal, $z(t) = 2\cos(\omega_1 + \omega_2)t$, is provided at input 106 to mixer 104. Note that the frequency, ω_1, is a shifting frequency that for the purposes of the present discussion can be a negative value. The Fourier transform, $Z(s)$, of the periodic signal, $z(t)$, is written as

$$Z(s) = \frac{2\pi}{\omega_1 + \omega_2}\mathrm{II}\left(\frac{\pi}{\omega_1 + \omega_2}s\right) = \frac{\pi}{\omega_1 + \omega_2}\left[\delta\left(\frac{\pi}{\omega_1 + \omega_2}s + \frac{1}{2}\right) + \delta\left(\frac{\pi}{\omega_1 + \omega_2}s - \frac{1}{2}\right)\right]$$

[0007] which can be rewritten as

$$Z(s) = \delta\left(s + \frac{\omega_1 + \omega_2}{2\pi}\right) + \delta\left(s - \frac{\omega_1 + \omega_2}{2\pi}\right).$$

[0008] Both the bandpass signal, $x(t)$, and the periodic signal, $z(t)$, are then provided to the inputs of mixer 104. The resulting signal, $e(t)$, at output 108 is therefore the product, $e(t) = x(t)z(t)$ whose Fourier transform is the convolution, $E(s) = X(s) * Z(s)$. From the above results for $X(s)$ and $Z(s)$ and after some mathematical manipulation, we have:

$$E(s) = X(s) * \delta\left(s + \frac{\omega_1 + \omega_2}{2\pi}\right) + \delta\left(s - \frac{\omega_1 + \omega_2}{2\pi}\right)$$

$$E(s) = X\left(s + \frac{\omega_1 + \omega_2}{2\pi}\right) + X\left(s - \frac{\omega_1 + \omega_2}{2\pi}\right)$$

$$E(s) = \tfrac{1}{2}F\left(s + \frac{2\omega_1 + \omega_2}{2\pi}\right) + \tfrac{1}{2}F\left(s - \frac{\omega_2}{2\pi}\right).$$

[0009] Thus, in the time domain, we have the inverse Fourier transform, $e(t)$, as

$$e(t) = f(t)\cos(2(\omega_1 + \omega_2)t) + f(t)\cos(\omega_2 t).$$

[0010] Note that the first term, $f(t)\cos(2(\omega_1 + \omega_2)t)$, is undesired and is therefore filtered out using filter 110. The output 112 of filter 110 is therefore

$$e'(t) = f(t)\cos(\omega_2 t).$$

[0011] Thus, the filtered output signal, e'(t), is a shifted version of the input signal, x(t).

[0012] Mixer 100 of Figure 1A can be used as part of a television tuner including single-conversion and dual-conversion television tuners for example. More recently, dual conversion tuners find wide application in television and cable tuners. In a dual conversion television tuner, as the name implies, two conversions (i.e., two mixers) are implemented. Moreover, in a dual conversion television tuner, the input frequency, $\omega_1+2\omega_2$, to bandpass filter 110 is referred to as an image frequency of the desired frequency, ω_1. The image frequency can sometimes be a problem and therefore may be filtered in such television tuner applications.

[0013] In a dual-conversion tuner 150, such as shown in Figure 1B, a first mixer 104 is implemented that up-converts a received RF signal, $x(t)$, at input 102 to a signal, $e(t)$, at mixer output 108 having a first intermediate frequency that is then filtered by filter 110 (note that like-numbered components between Figure 1A and Figure 1B operate similarly). The filtered signal, $e'(t)$, at input 112 to mixer 114 is then at a nominal amplitude while all the rejected signals are at a much lower amplitude. The filtered signal, $e'(t)$, is then input to a second mixer 114 where mixer 114 mixes signal $y(t)$ at input 116 to down-convert the filtered signal, $e'(t)$, into a desired IF signal, $m(t)$, at output 118. The desired IF signal, $m(t)$, is thus the channel a user wishes to view. In actual implementation, amplification of signals and other factors need to be considered as will be discussed below.

[0014] Using the techniques described above, a prior art tuner 200 is built as shown in Figure 2. Tuner 200 includes dual mixers 202 and 204 similar in operation to those mixers 104 and 114 described with reference to Figure 1b. Dual mixers 202 and 204 receive local oscillator signals from local oscillators LO1 264 and LO2 268 at mixer inputs 206 and 208, respectively. Oscillator circuit 210 is configured to drive local oscillators LO1 264 and LO2 268 responsive to external clock signal 212 generated by crystal 214. As shown in Figure 1, crystal 214 generates external clock signal 212 with a frequency of 5.25 MHz. External clock signal 212 is then directed to reference frequency

generator 240 which generates a reference signal for phased lock loop PLL1 220 of oscillator circuit 210 which is configured to provide input signal 262 to local oscillator LO1 264. External clock signal 212 is further directed to reference frequency generator 216. Using external clock signal 212 with a frequency of 5.25 MHz, reference frequency generator generates reference signal 218 operating at 2.625 MHz. Reference signal 218 is then directed to oscillator circuit 210 and, more particularly, to phase locked loop PLL2 228. Using the reference signal 218, phase locked loop PLL2 228 is configured to provide signal 266 to local oscillator LO2 268.

[0015] Tuner 200 can be configured to operate in television systems where, for example, signals representing individual channels are assigned to specific frequencies in a defined frequency band. Illustratively, in the United States, television signals are generally transmitted in a band from 55 MHz to 806 MHz. Such a radio frequency (RF) signal can, therefore, be received at input 230 of tuner 200. The received RF signal passes through a front-end filter 232 that filters out any signals outside of the frequency range of interest (i.e., outside of 55MHz to 806 MHz). Filter 100 can be a bandpass filter or, more typically, a low pass filter that is designed to remove all frequencies above an input cutoff frequency, ω_c. The input cutoff frequency, ω_c, is chosen to be higher than the frequencies of the channels in the television band. The output 234 of filter 100 is then directed to amplifier 236 to provide the signal (238) that is then directed to mixer input 238 of mixer 202. As described above, mixer 202 also receives at input 206 a local oscillator signal from local oscillator LO1 264.

[0016] The output 238 of mixer 202 is a first intermediate frequency signal IF1 which is directed to IF filter 244. Typically, the frequency of local oscillator LO1 264 is variable and selected responsive to a desired channel in the RF signal at input 230. Moreover, the frequency local oscillator LO1 264 is selected such that mixing of the local oscillator signal at input 206 and the filtered and amplified signal at mixer input 238 generates signal IF1 at a specified frequency or within a narrow range of frequencies as may be desired. IF filter 244 is a band pass filter that is used to remove unwanted frequencies and spurious signals from the signal IF1. The output of IF filter 244 is then directed to

mixer input 246 of mixer 204 which also receives a second local oscillator signal at input 208 that is generated by local oscillator LO2 268. Mixer 204 is configured to mix such signals to generate a second intermediate frequency signal, IF2, which is then directed to input 248 of amplifier 250. In television tuner applications, mixer 204 may be an image rejection mixer that rejects image frequencies from the second intermediate frequency signal, IF2.

[0017] Local oscillator signal LO2 268 can be configured to generate a variable or fixed frequency signal depending upon whether the first intermediate frequency signal, IF1, is at a fixed frequency or if it varies over a range of frequencies. Regardless, the frequency of the signal generated by local oscillator LO2 268 is selected to generate a fixed frequency signal IF2 that is directed to input 248 of amplifier 250. Output 252 of amplifier 250 is, therefore, amplified signal IF2' that is directed to additional processing circuitry 254 to generate either digital or analog television signals as may be desired. Further included in tuner 100 is serial control circuitry 256. Among other things, serial control circuitry 256 controls phased locked loops PLL1 and PLL2 to set the frequencies of local oscillators LO1 264 and LO2 268.

[0018] Advances have been made to integrate much circuitry into a single integrated circuit. Prior art applications typically integrate the circuitry enclosed by box 258. Notably, front end filter 232 and IF filter 244 are typically placed outside of an integrated circuit. This is not surprising because of the size and other design considerations of such filters. The present invention, however, teaches a manner for integrating IF filter 244 onto a tuner IC.

SUMMARY

[0019] In one embodiment, the invention is an intermediate frequency filter for use in an integrated circuit. The filter includes a first filter stage, the first filter stage including a first LC resonator. The first filter stage further includes a first adjustable capacitor array coupled to the first LC resonator. The first adjustable capacitor array has an effective capacitance value adjustable through use of a first plurality of programmable data storage

locations. The first plurality of programmable data storage locations are programmable through a serial control interface.

[0020] In an alternate embodiment, the invention is a circuit formed as part of a single integrated circuit. The circuit includes a first amplifier, a first oscillator, and a first mixer coupled to the first amplifier and the first oscillator. The circuit also includes a second oscillator, a second mixer coupled to the second oscillator, and a second amplifier coupled to the second mixer. The circuit further includes a serial control module and an intermediate frequency filter (IF filter). The IF filter includes a first filter stage, the first filter stage including a first LC resonator. The first filter stage further includes a first adjustable capacitor array coupled to the first LC resonator. The first adjustable capacitor array has an effective capacitance value adjustable through use of a first plurality of fuses, the first plurality of fuses programmable through the serial control module. The second mixer is coupled to the IF filter and the IF filter is coupled to the first mixer. Note that the various components may or may not all be formed on the integrated circuit. For example, an inductor of an LC resonator may be formed outside the integrated circuit and coupled to the integrated circuit.

[0021] In another alternate embodiment, the invention is a method of tuning an integrated circuit. The method includes receiving an integrated circuit having therein an intermediate filter with a first tunable capacitive array. The method further includes testing the integrated circuit. The method also includes adjusting the first tunable capacitive array responsive to the testing, to effect a change in a frequency response of the intermediate filter. The method also includes repeating the testing and the adjusting as needed to achieve a desired frequency response of the intermediate filter.

[0022] In yet another alternate embodiment, the invention is a method of tuning an integrated circuit during operation. The invention includes operating the integrated circuit. The invention also includes adjusting a tunable capacitive array to effect a change in frequency response of an intermediate filter.

[0023] In yet another alternate embodiment, the invention is an apparatus. The apparatus includes a means for filtering an intermediate frequency signal on an integrated circuit.

The apparatus also includes a first means for adjusting a response of the means for filtering. The apparatus further includes a means for programming the first means for adjusting.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. The drawings should be understood as illustrative of the invention, rather than restrictive.

[0025] Figure 1A is a block diagram of an embodiment of a system for up-converting a signal at a first frequency to an intermediate frequency.

[0026] Figure 1B is a block diagram of an embodiment of a dual conversion system for up-converting a signal at a first frequency to a first intermediate frequency and then down-converting the first intermediate frequency to a second frequency.

[0027] Figure 2 is a block diagram of an embodiment of a dual-conversion tuner with an external IF filter according to the prior art.

[0028] Figure 3 is a schematic of an embodiment of a switched capacitor resonator that tunes a fixed value LC resonator by coupling and decoupling various capacitors.

[0029] Figure 4 is a block diagram of an embodiment of a circuit configured to set the tuning of a switched capacitor resonator.

[0030] Figure 5 is a block diagram of an embodiment of an integrated dual-conversion tuner with a switched capacitor resonator configured to perform IF filtering.

[0031] Figure 6 is a block diagram of an alternate embodiment of an integrated dual-conversion tuner with a switched capacitor resonator configured to perform IF filtering.

[0032] Figure 7 is a schematic of an alternate embodiment of an IF filter.

[0033] Figure 8 is a flow diagram of an embodiment of a method of tuning an IF filter.

[0034] Figure 9 is a flow diagram of an alternate embodiment of a method of tuning an IF filter.

DETAILED DESCRIPTION

[0035] In order to understand the present invention, it is useful to understand a tuner according to the prior art. Multiplying a lowpass signal by a high-frequency periodic signal translates the spectrum of the lowpass signal to all frequencies present in the periodic signal. Quite often it is desirable to translate a bandpass signal to a new center frequency. This process can be accomplished by multiplication of the bandpass signal by a periodic signal and is called mixing or converting.

[0036] In one embodiment, the invention is an intermediate frequency filter for use in an integrated circuit. The filter includes a first filter stage, the first filter stage including a first LC resonator. The first filter stage further includes a first adjustable capacitor array coupled to the first LC resonator. The first adjustable capacitor array has an effective capacitance value adjustable through use of a first plurality of programmable data storage locations. The first plurality of programmable data storage locations are programmable through a serial control interface.

[0037] In an alternate embodiment, the invention is a circuit formed as part of a single integrated circuit. The circuit includes a first amplifier, a first oscillator, and a first mixer coupled to the first amplifier and the first oscillator. The circuit also includes a second oscillator, a second mixer coupled to the second oscillator, and a second amplifier coupled to the second mixer. The circuit further includes a serial control module and an intermediate frequency filter (IF filter). The IF filter includes a first filter stage, the first filter stage including a first LC resonator. The first filter stage further includes a first adjustable capacitor array coupled to the first LC resonator. The first adjustable capacitor array has an effective capacitance value adjustable through use of a first plurality of fuses, the first plurality of fuses programmable through the serial control module. The second mixer is coupled to the IF filter and the IF filter is coupled to the first mixer.

[0038] In yet another alternate embodiment, the invention is an apparatus. The apparatus includes a means for filtering an intermediate frequency signal on an integrated circuit. The apparatus also includes a first means for adjusting a response of the means for

filtering. The apparatus further includes a means for programming the first means for adjusting.

[0039] Note that the various components may or may not all be formed on the integrated circuit. For example, an inductor of an LC resonator may be formed outside the integrated circuit and coupled to the integrated circuit in some embodiments. In such embodiments, the presence of the adjustable (switched) capacitive array on the integrated circuit may be used to compensate for variations in the off-IC inductor and connections to the off-IC inductor. Forming inductors is notoriously difficult, so allowing for a separate substrate for inductors is a potentially cost-saving option. Inductors may be formed with thick metal on various substrates, whether integrated with the rest of an IC or on a separate substrate or printed circuit board. In some embodiments, all of the integrated circuits are formed on silicon on insulator substrates, while other embodiments use other substrates.

[0040] In another alternate embodiment, the invention is a method of tuning an integrated circuit. The method includes receiving an integrated circuit having therein an intermediate filter with a first tunable capacitive array. The method further includes testing the integrated circuit. The method also includes adjusting the first tunable capacitive array responsive to the testing, to effect a change in a frequency response of the intermediate filter. The method also includes repeating the testing and the adjusting as needed to achieve a desired frequency response of the intermediate filter.

[0041] In yet another alternate embodiment, the invention is a method of tuning an integrated circuit during operation. The invention includes operating the integrated circuit. The invention also includes adjusting a tunable capacitive array to effect a change in frequency response of an intermediate filter.

[0042] The present invention, in one embodiment, provides a bandpass filter comprising integrated, fixed value inductors and capacitors with electronically controlled, switchable capacitors having a binary weighting. Such capacitors are used to correct for fixed-component variations and to provide a variable passband response. As will be described, a binary weighting is used for reduced complexity and increased range in tuning. The

invention, in one embodiment, is used to create an accurate bandpass filter having reduced passband bandwidth and improved image rejection performance while also reducing the insertion loss of the bandpass filter.

[0043] The implementation of switched-capacitor elements allows for correction of fixed element tolerances which cannot be avoided. For example, inductors and capacitor values are typically provided with an identified tolerance (e.g., 10 % tolerance) such that, when implemented in a circuit, the accumulation of tolerance errors cannot be accurately predicted. The switched-capacitor elements of the present invention allow for the correction of filter performance and response that may be affected by fixed element tolerances. When used with an image rejection mixer, the present invention provides a major advantage over the prior art by eliminating an expensive external IF filter such as filter 244 of Figure 2.

[0044] The present invention is appropriate for use in over-the-air television applications as well as broadband cable tuner applications. Furthermore, the present invention has many other applications where costly or undesirable external filters are used in receiver or transmitter systems. Note that an entire external filter is different from external components which make up part of an internal filter. For example, in some embodiments, an inductor may be external to the rest of an integrated internal filter, yet be part of the LC resonator of such a filter. In other embodiments, such an inductor may be formed as part of the same integrated circuit on the same substrate as the rest of an internal filter.

[0045] As a starting point, a simple filter including a switched capacitive array is illustrated. With reference to Figure 3, there is shown a switched capacitor resonator 300 that includes a fixed LC resonator 301 coupled to various switched capacitors 306 through 314. As shown inductor 302 in combination with capacitor 304 collectively form a resonator with an associated time constant. The production of integrated circuits and in particular, integrated tuners, introduces significant variance in component values especially in high-Q inductors. Importantly, in some embodiments, fixed LC resonator 301 of the present invention provides high-Q inductors by placing a thick layer of metal

on a top-most layer of semiconductor die when using an insulating type wafer (such as MBIC-20 for example). Production of an integrated circuit with inductor 302 and capacitor 304 can be designed for a particular value, however, in actual implementation a slightly different time constant may be required for optimal operation. Thus, in an embodiment of the invention, switched capacitors 306 through 314 are provided as an adjustment to fixed LC resonator 301. Similarly, in some embodiments, it may be useful to provide an external inductor as inductor 302, in which case the variable aspect of inductance will result from a combination of variations in inductor 302 and variations in connections to inductor 302.

[0046] In Figure 3, switched capacitor 306 is illustrated including several components such as capacitors 316 through 322 and transistor 324. Transistor 324 is preferably operated as a binary device that is either in the fully on state or the fully off state. In the on state, transistor 324 provides a low impedance connection between capacitors 318 through 320. Moreover, in such a state, capacitors 316 through 322 become coupled to fixed LC resonator 301. Series coupled capacitors 316 through 322, each with value C_1 produces an equivalent capacitance of $\frac{1}{4}$ C_1. Moreover, series coupled capacitors 316 through 322 become coupled in parallel to the capacitor 304. Where capacitor 304 has a capacitance of C, the resulting equivalent capacitance becomes $C+\frac{1}{4}$ C_1. Moreover, the time constant of the switched capacitor resonator 300 is modified in a known way. When transistor 324 is in the off state, capacitors 316 through 322 are de-coupled from fixed LC resonator 301 and, therefore, do not have a significant effect on its time constant. Thus, transistor 324 can be used to change the time constant of fixed LC resonator 301 in a known way.

[0047] The operation of switched capacitors 308 through 314 is similar to switched capacitor 306. Importantly, however, the associated capacitive contributions of switched capacitors 308 through 314 are $\frac{1}{2}$ C_1, C_1, $2C_1$ and $4C_1$, respectively. With these capacitive values, there is provided a wide range of adjustment to fixed LC resonator 301. In one embodiment, more similarly configured switched capacitors (not shown) are provided to allow a wider range of adjustment to fixed LC resonator 301. In another

embodiment , resistors 360 through 378 are provided to allow further adjustment to fixed LC resonator 301. In another embodiment, resistors 360 through 378 are provided to provide dissipation of charge from the capacitors to which they are coupled.

[0048] In another embodiment of the invention, shown in Figure 4, switched capacitor resonator 400 includes fixed LC resonator 402 and switched capacitor array 404 including various switched capacitors as described with reference to Figure 3. Moreover, switched capacitor resonator 400 further includes adjustable capacitor array 406 in order to compensate switched capacitor 400 for beat issues. Adjustable capacitor array 406 is configured in a similar manner to switched capacitor array 404, but can be configured to provide different ranges of adjustment for frequencies and time constants of interest. Adjustable capacitor array 406 is provided for situations where a beat frequency produced in conjunction with other circuitry, is closely centered about the center frequency of switched capacitor resonator 400. In general, switched capacitor array 404 is provided to account for variation in component tolerances and adjustable capacitor array 406 is provided to account for beating or other circuit-specific issues. Switched capacitor arrays can be used in other ways to account for issues arising in many other applications.

[0049] Further shown in Figure 4 are switch lines 408 through 416 which respectively correspond to switch lines 350 through 358 of Figure 3 that control the states of transistors 324, 330, 336, 342, and 348. Through measurements and tests, an appropriate combination of switched capacitors can be determined that tunes Fixed LC resonator 402. Having determined an appropriate combination, it is desirable to permanently set or "hard wire" the appropriate combination. In an embodiment of the invention, permanently setting the appropriately chosen switched capacitors is achieved through blowing or not blowing appropriately chosen fuses of fuses 418 through 426. In this manner, transistors of each switched capacitor are set either on or off as desired. In an embodiment of the invention, serial test and fix control unit 428 is used to test and fix (set) the fuses 418 through 426 in an appropriate state.

[0050] One example of a serial control interface is the inter-IC (I^2C) bus, a two-wire serial bus used to control inter-integrated circuit operations. One wire is the Serial Clock Line (SCL), and the other is the Serial Data Line (SDL). The bus is controlled by a bus master device that tells slave devices when they can access the bus. Each slave has a unique 7-bit or 10-bit address. When the master device accesses a slave, it sends the address and a read/write bit. Then, the addressed slave acknowledges the connection and the master can send or receive data to or from the slave. Other serial interfaces may be appropriate, and parallel or serial-parallel interfaces may be appropriate, too.

[0051] With fixed LC resonator 402 tuned to compensate for variations in inductor and capacitor values it may still be necessary to tune fixed LC resonator 402 to compensate for beating issues. Beating, that is the constructive and destructive interaction of two signals of different frequency, can become a significant issue when implementing an integrated tuner of the present invention with other electronic components. Where the beat frequency is equal to the absolute value of the difference in frequency of two signals, switched capacitor resonator 400 can be further configured to reduce or eliminate such beating. In another embodiment of the invention, as shown in Figure 4, switched capacitor resonator 400 further includes adjustable capacitor array 404 which includes various switched capacitors similar to those described with reference to Figure 3. Adjustments necessary to reduce or eliminate beating can be much different than adjustments associated with IF filtering issues. Accordingly, the range of adjustment of adjustable capacitor array 406 can be significantly different from the range of switched capacitor array 404; however, the general characteristics are similar. To set adjustable capacitor array 406, it is coupled to control lines 430 and 432. Moreover, fuses 434 and 436 may be provided for permanently setting the configuration of adjustable capacitor array 406. Serial bandpass control unit 438 is provided for setting fuses 434 and 436 as necessary.

[0052] Alternatively, in some embodiments, fuses 434 and 436 may be substituted for some other form of programmable storage location, such as an EEPROM cell, EPROM cell, ROM cell, flip-flop, or bits of a register for example. Similarly, it may be

appropriate to use an alternative form of storage location for fuses 418 through 426. Also, various embodiments of the switched capacitive arrays may utilize more or fewer capacitors and associated transistors, allowing for different tuning resolutions and design requirements, and requiring a different number of control lines. Furthermore, note that in some embodiments, a lookup table of values may be used for purposes of programming one of the switched capacitive arrays, allowing for programming based on expected performance or characteristics of the overall system and for rapid programming responsive to predetermined conditions.

[0053] As previously described, IF filters are typically not integrated within an integrated tuner for various reasons. One reason is that tuning of the IF filter is usually necessary. Because the filter of the present invention solves the tuning problem, it can, therefore, be more readily integrated with a tuner. Shown in Figure 5 is tuner 500 that includes switched capacitor resonator-based IF filter 504 within integrated tuner 560. Significant features of integrated tuner 560 include mixers that operate similarly to mixers 202 and 204 of Figure 2. Importantly, however, switched capacitor resonator 504, coupled between mixers 502 and 506, operates as an IF filter similar to filter 244 of Figure 2. Also, serial control circuitry 556 operates similarly to serial control circuitry 256 of Figure 2, however, because of the increased functionality of integrated tuner 500, and in particular, filter 504, serial control circuitry further includes appropriate controls for filter 504.

[0054] The switched capacitor resonator of the present invention can, therefore, operate as a filter and, in particular, as a bandpass filter appropriate for use in a television tuner. The switched capacitor resonator, or filter, of the present invention is tuned by measuring response characteristics at the various settings of a switched capacitor array. In measuring a television signal, for example, both within the desired passband and at the image frequency, it is possible to determine an optimal setting for the switched capacitor array. In one embodiment, the switched capacitor array is provided with fuse links that can be set or "blown" to fix the desired response of the bandpass filter of the present invention.

[0055] In another embodiment, an inter-stage amplifier is added such that two or more filters can be used to achieve additional rejection of unwanted signals. These filters can be identical or different and have independently controlled capacitor arrays to further improve the response of the tuner.

[0056] In yet another embodiment of the invention, a second switched capacitor array is provided that can be controlled by the user to provide further tuning capability. This embodiment provides for the avoidance of known difference beat products that fall within a desired channel. Moreover, this added control allows for the integration on a single integrated circuit of two local oscillators LO1 544 and LO2 548, as shown in Figure 5, while maintaining acceptable performance. Local oscillators LO1 544 and LO2 548 are configured as voltage controlled oscillators (VCOs) that receive appropriate control signals from dual synthesizer 508.

[0057] As shown integrated tuner 560 is further provided with filter 510 and amplifier 514 for meeting case linearity requirements. As shown, amplifier 514 buffers filtered integrated tuner output signal 540 to generate output signal 516. To complement the automatic gain control 526 of amplifier 524, amplifier 514 can also be provided with automatic gain control 562.

[0058] As discussed, alternate embodiments may be suitable for implementation. Figure 6 illustrates an alternate embodiment of a tuner which utilizes an IF filter including a switched capacitor array. Tuner 600 includes an amplifier, an upconversion stage, an IF filter, a downconversion stage, another amplifier, a bandpass filter, and yet another amplifier. Amplifier 605 includes variable (automatic) gain control and receives an input signal. Coupled to the output of amplifier 605 is mixer 610, which also receives an output from oscillator 620. Oscillator 620 and oscillator 630 are controlled by dual synthesizer 625, which causes the oscillators 620 and 630 to output desired frequency signals.

[0059] High IF filter 615 receives the output of mixer 610 (the output of amplifier 605 mixed with the signal from local oscillator 620). Filter 615 is an intermediate frequency filter implemented with an LC resonator and one or more switched capacitor arrays for

trimming. As such, filter 615 may be tuned to reject beats associated with the combination of oscillators 620 and 630 and may be tuned to respond appropriately despite variations in the inductor and capacitor of the included LC resonator.

[0060] The output of filter 615 is coupled to mixers 640 and 635. Mixer 640 receives the 0° phase of the output of oscillator 630 from quadrature generator 645, while mixer 635 receives the 90° phase of the output of oscillator 630 from quadrature generator 645. The outputs of mixers 635 and 640 are coupled to delay lines 655 and 650 respectively, which pass through the 0° phase and delay the 90° phase by an additional 90° before the two signals are then summed at adder 660. The output of adder 660 is provided to the amplifier 665, and, in amplified form, is passed through bandpass filter 670 to another amplifier 675 which has a variable gain control included. Note that the combination of quadrature generator 645, mixers 635 and 640, delay lines 650 and 655, and adder 660 make up a common image rejection mixer, thus indicating that IF filter 615 may or may not need to include an image rejection stage. Other image rejection mixers or filter stages may be appropriate in other embodiments.

[0061] In some embodiments, the input of the above system is the compound signal from a coaxial cable or antenna and the output of the above system may be expected to be a television signal which may be utilized to provide a digital or analog television picture. In such instances, the IF filter 615 may be implemented as a filter such as that illustrated in Figure 7. Alternatively, a filter such as that illustrated in Figure 3 may be utilized.

[0062] Illustrated in Figure 7 is an alternate embodiment of a filter including switched capacitor arrays. Filter 700 of Figure 7 may be understood as a two stage filter, with a bandpass stage and an image rejection stage, and with amplifiers at the input, intermediate and output positions of filter 700. Module 705 is an initial amplifier which may be used for isolation purposes, may be used to automatically adjust the magnitude of a signal and terminate (impedance match) the signal, and may also be used to strengthen a signal which is expected to lose strength within the filter. Modules 715, 725 and 735 are distinct LC resonators including a capacitor and an inductor, and each of which includes a switched capacitor array as represented by the variable capacitance. In one

embodiment, the combination of modules 715, 725 and 735 implement a bandpass filter with relatively low image rejection and loss characteristics.

[0063] Moreover, in one embodiment, capacitors 712 and 717 are selected with a predetermined value which, through coupling two non-adjacent modules (715 and 735), implement an image trap. The image trap provides for image rejection (a transmission zero or near-zero) at a predetermined frequency based on the predetermined value of the capacitors. Note that the predetermined value of these capacitors 712 and 717 may be determined within a relatively wide tolerance, thus allowing the system designer to avoid attempting to tightly constrain the capacitance values in question and to avoid including circuitry suitable for adjusting these capacitance values.

[0064] Coupled to the output of modules 715, 725 and 735 is intermediate stage amplifier 745, which further boosts the signal and terminates both the bandpass filter stage and the image rejection stage. Coupled to the output of amplifier 745 are modules 755, 765 and 775. Each of modules 755, 765 and 775 are distinct LC resonators including a capacitor and an inductor, and each of which includes a switched capacitor array as represented by the variable capacitance. In one embodiment, the combination of modules 755, 765 and 775 implement an image rejection filter with relatively high image rejection including a notch at a predetermined image frequency and relatively high loss characteristics compared to the bandpass filter of modules 715, 725 and 735. Also, in one embodiment, capacitors 772 and 777 are selected with a predetermined value which, through coupling two non-adjacent modules (755 and 775), implement an image trap. The output of the image rejection filter is coupled to amplifier 785, which provides the output of the overall filter and terminates the image rejection filter stage.

[0065] In some embodiments, the input to a tuner is on a 45.75 MHz carrier which is then mixed with a significantly higher frequency carrier (Frequency X) prior to input to the IF filter. One result of this mixing is an undesired image of the input signal at a frequency twice the carrier (91.5 MHz) below the higher frequency carrier, or an image at X-91.5 MHz. Rejecting this frequency even at a cost of higher then desirable loss characteristics may thus be valuable, and the image rejection filter of modules 755, 765 and 775 may be

useful for this purpose. In such an instance, the bandpass filter of modules 715, 725 and 735 may be useful for reducing noise from other sources, while providing a relatively low level of insertion loss. However, alternate embodiments may be implemented in which only a single filter stage or some other arrangement is used. In each embodiment, the presence of one or more switched capacitor arrays may be useful for tuning the filter in question based on manufacturing and customization variations in the underlying system design.

[0066] Note that the embodiment illustrated in Figure 7 uses a balanced approach. However, a single-ended approach may also be appropriate in some instances. An otherwise unbalanced approach may have merits due to various design constraints, too. Also, note that the capacitors coupling the adjacent modules or tanks of the filter stages may be implemented with appropriate capacitances values having large tolerances relative to the tolerances for the capacitance of the LC resonator.

[0067] The methods implemented by the various embodiments may be classified into two general areas, manufacturing methods and operational methods. Figure 8 is a flow diagram of an embodiment of a method of tuning an IF filter. Method 800 of Figure 8 is a manufacturing method useful for tuning a filter based on process and component variations within expected tolerances. At operation 810, a tunable filter (separately or as part of a system) is received. At operation 820, the filter is tested to determine its current characteristics or operational profile. At operation 830, the filter is tuned to an operational profile closer to a predetermined operational profile. At operation 840, a determination is made as to whether the filter is sufficiently well tuned, as to whether its operational profile or response is within predetermined limits. If not, the process returns to operation 820. If the filter is sufficiently well tuned, at operation 850 the filter may be completed, such as by writing a serial number or validation code into an associated internal ID register for example. Such a completion operation may not be necessary, the filter may effectively be manufactured and tested when tuning is complete.

[0068] After manufacture, the filter may be used within a system which has different characteristics than the expected nominal characteristics for which it was designed.

Figure 9 is a flow diagram of an alternate embodiment of a method of tuning an IF filter. Method 900 of Figure 9 is exemplary of an operational method of tuning an IF filter. At operation 910, the filter is operated. At operation 920, the frequency used in the overall system is shifted. At operation 930, the filter characteristics are shifted responsive to the shift of operation 920. Such a shift may result from changing a channel in a set-top box for example, or may result from shifts in operating characteristics of other components within a system for example. Note that the method illustrated may be repeated as needed during operation of the filter. Note also that the shift in filter characteristics may be effected by programming values from a lookup table into a register for example, thereby allowing for predetermined responses to expected changes in operating conditions. Alternatively, some variant of trial and error may be used to determine a preferred tuning status for the filter, based on changes to the filter and observed performance.

[0069] From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the spirit and scope of the invention. In some instances, reference has been made to characteristics likely to be present in various or some embodiments, but these characteristics are also not necessarily limiting on the spirit and scope of the invention. In the illustrations and description, structures have been provided which may be formed or assembled in other ways within the spirit and scope of the invention. Similarly, methods have been illustrated and described as linear processes, but such methods may have operations reordered or implemented in parallel within the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

IN THE CLAIMS

We claim:

1. An intermediate frequency filter for use in an integrated circuit, comprising:

a first filter stage, the first filter stage including a first LC resonator; and

the first filter stage further including a first adjustable capacitor array coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of programmable data storage locations, the first plurality of programmable data storage locations programmable through a serial control interface.

2. The filter of claim 1, wherein:

the first filter stage further including a second adjustable capacitor array coupled to the LC resonator, the second adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of data storage locations, the second plurality of data storage locations programmable through the serial control interface.

3. The filter of claim 2, wherein:

the data storage locations of the second plurality of data storage locations are fuses.

4. The filter of claim 2, wherein:

the data storage locations of the second plurality of data storage locations are bits of a register.

5. The filter of claim 1, wherein:

the first capacitive array includes a first capacitor of a first magnitude coupled in series with a first switch and further coupled in series with a second

capacitor of the first magnitude, the switch controlled by a first fuse of the first plurality of fuses; and

the first capacitive array includes a third capacitor of a second magnitude coupled in series with a second switch and further coupled in series with a fourth capacitor of the second magnitude, the switch controlled by a second fuse of the first plurality of fuses, the combination of the third capacitor, second switch and fourth capacitor coupled in parallel with the combination of the first capacitor, first switch and second capacitor.

6. The filter of claim 1, further comprising:

a second filter stage coupled to the first filter stage, the second filter stage including a second LC resonator; and

the second filter stage further including a third adjustable capacitor array coupled to the second LC resonator, the third adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of fuses, the second plurality of fuses programmable through the serial control interface.

7. The filter of claim 6, further comprising:

an amplifier, the amplifier coupled to the first filter stage to receive an output of the first filter stage, the amplifier coupled to the second filter stage to provide an input to the second filter stage.

8. A circuit formed as part of a single integrated circuit, the circuit comprising:

a first amplifier;

a first oscillator;

a first mixer coupled to the first amplifier and the first oscillator;

a second oscillator;

a second mixer coupled to the second oscillator;

a second amplifier coupled to the second mixer;

a serial control module;

an intermediate frequency filter (IF filter), the IF filter including a first filter stage, the first filter stage including a first LC resonator;

the first filter stage further including a first adjustable capacitor array coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of fuses, the first plurality of fuses programmable through the serial control module;

and wherein the second mixer is coupled to the IF filter and the IF filter is coupled to the first mixer.

9. The circuit of claim 8, wherein the first filter stage further includes

a second adjustable capacitor array coupled to the LC resonator, the second adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of data storage locations, the first plurality of data storage locations programmable through the serial control module.

10. The circuit of claim 9, further comprising:

a second filter stage coupled to the first filter stage, the second filter stage including a second LC resonator;

the second filter stage further including a third adjustable capacitor array coupled to the second LC resonator, the third adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of fuses, the second plurality of fuses programmable through the serial control module; and

the second filter stage further including a fourth adjustable capacitor array coupled to the LC resonator, the fourth adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of data storage locations, the second plurality of data storage locations programmable through the serial control module.

11. The circuit of claim 10, further comprising:

a third amplifier, the third amplifier coupled to the first filter stage to receive an output of the first filter stage, the third amplifier coupled to the second filter stage to provide an input to the second filter stage.

12. The circuit of claim 11, further comprising:

a dual synthesizer coupled to the first oscillator and the second oscillator.

13. A method of tuning an integrated circuit, comprising:

receiving an integrated circuit having therein an intermediate filter with a first tunable capacitive array;

testing the integrated circuit;

adjusting the first tunable capacitive array responsive to the testing, to effect a change in a frequency response of the intermediate filter; and

repeating the testing and the adjusting as needed to achieve a desired frequency response of the intermediate filter.

14. The method of claim 13, further comprising:

operating the integrated circuit; and

adjusting a second tunable capacitive array to effect a change in frequency response of the intermediate filter.

15. The method of claim 14, wherein:

adjusting the second tunable capacitive array includes programming the second tunable capacitive array based on a lookup table.

16. The method of claim 15, further comprising:

constructing the lookup table responsive to the testing.

17. The method of claim 14, wherein:

adjusting the second tunable capacitive array includes internally measuring the frequency response of the intermediate filter.

18. A method of tuning an integrated circuit during operation, comprising:

operating the integrated circuit; and

adjusting a tunable capacitive array to effect a change in frequency response of an intermediate filter.

19. The method of claim 18, further comprising:

detecting a change in an operating frequency of the integrated circuit; and wherein the adjusting occurs responsive to the detecting.

20. The method of claim 18, wherein:

adjusting the tunable capacitive array includes programming the tunable capacitive array based on a lookup table.

21. The method of claim 18, wherein:

adjusting the second tunable capacitive array includes internally measuring the frequency response of the intermediate filter.

22. An apparatus, comprising:

means for filtering an intermediate frequency signal on an integrated circuit;

first means for adjusting a response of the means for filtering; and

means for programming the first means for adjusting.

23. The apparatus of claim 22, further comprising:

second means for adjusting the response of the means for filtering.

24. The apparatus of claim 23, further comprising:

means for repeatedly programming the second means for adjusting.

ABSTRACT

In one embodiment, the invention is an intermediate frequency filter for use in an integrated circuit. The filter includes a first filter stage, the first filter stage including a first LC resonator. The first filter stage further includes a first adjustable capacitor array coupled to the first LC resonator. The first adjustable capacitor array has an effective capacitance value adjustable through use of a first plurality of data storage locations. The first plurality of data storage locations are programmable through a serial control interface.

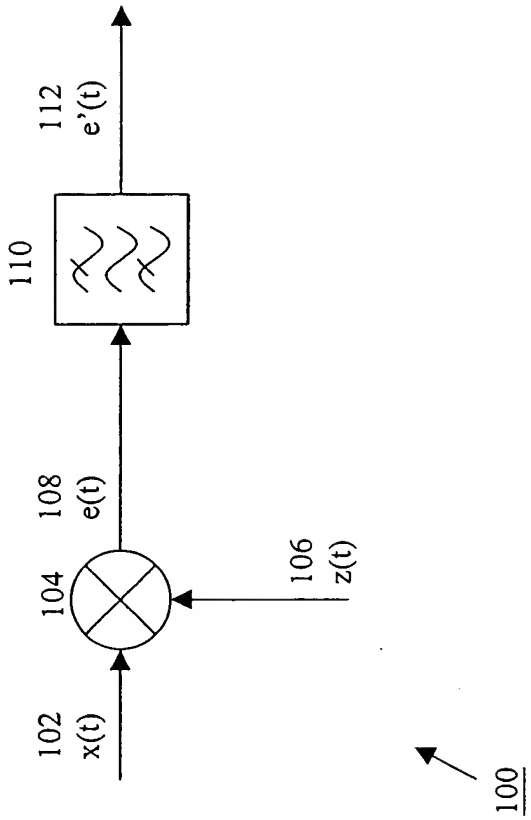


Figure 1A

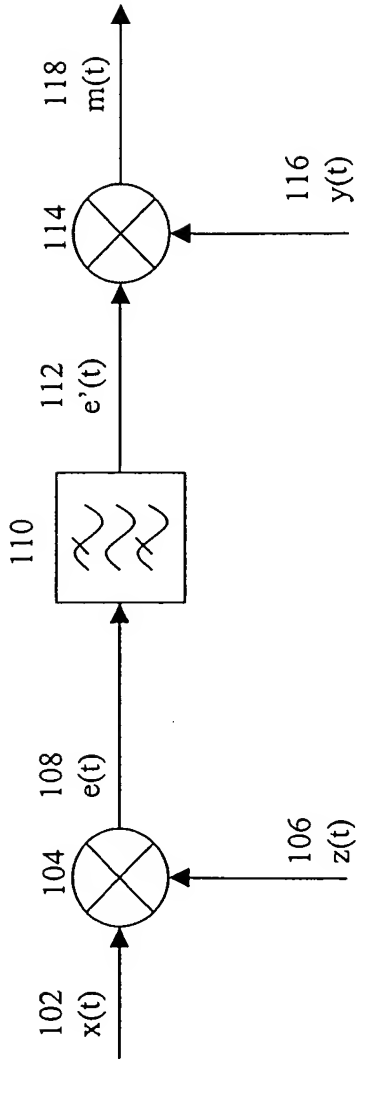
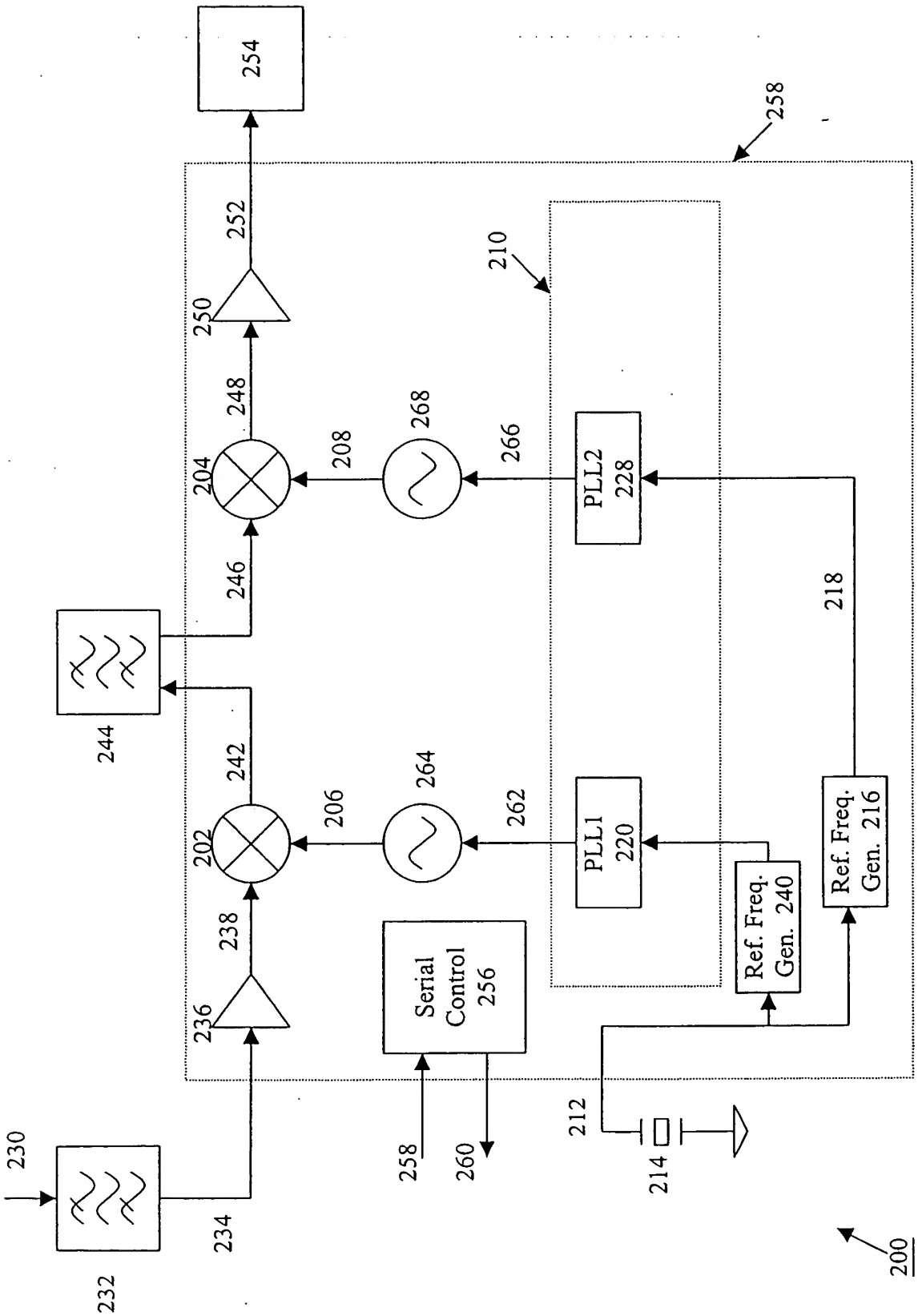


Figure 1B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202
PLL1
220
238
Serial
Control
256
Ref. Freq.
Gen. 240
Ref. Freq.
Gen. 216
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200

Figure 2

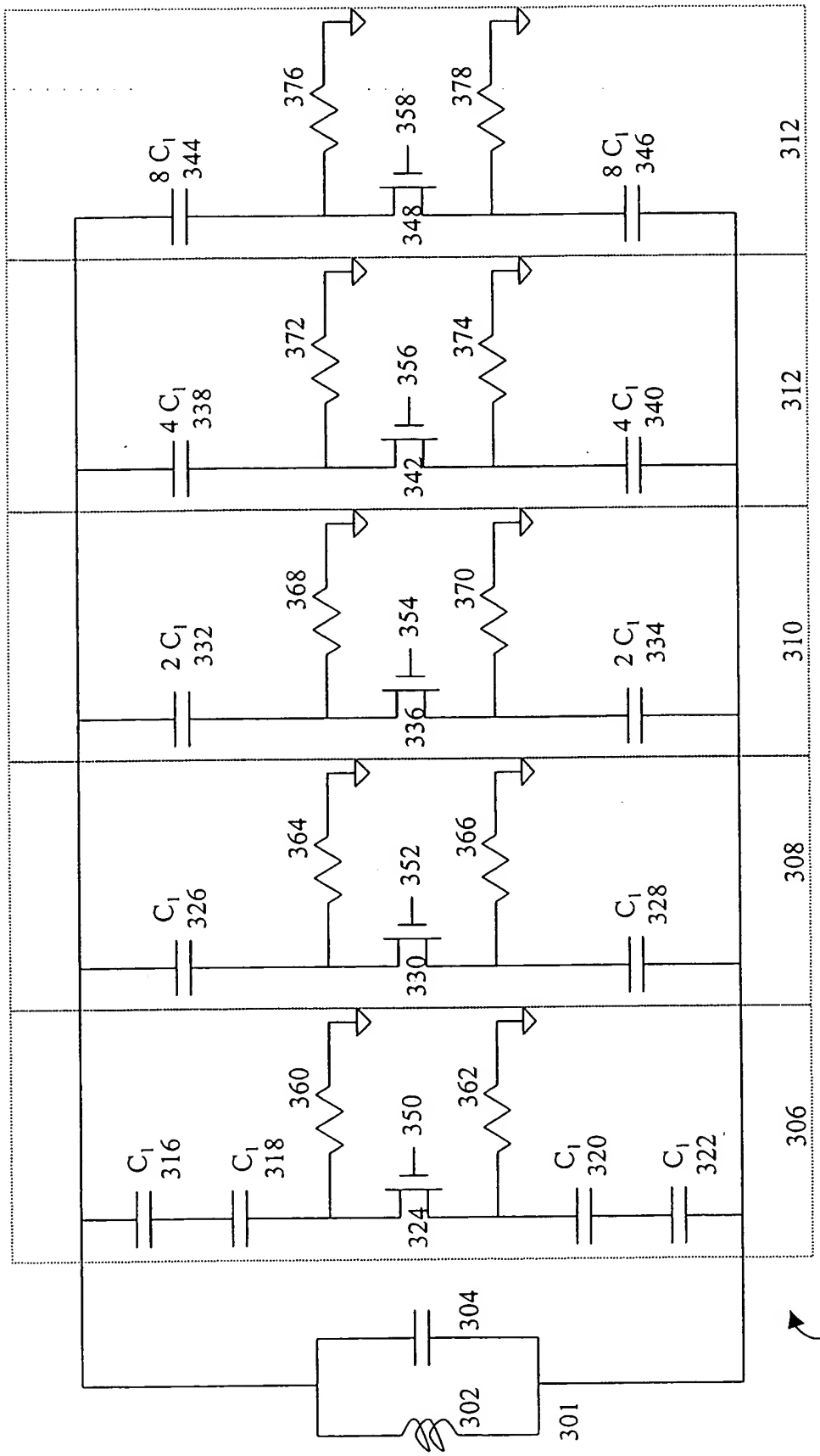
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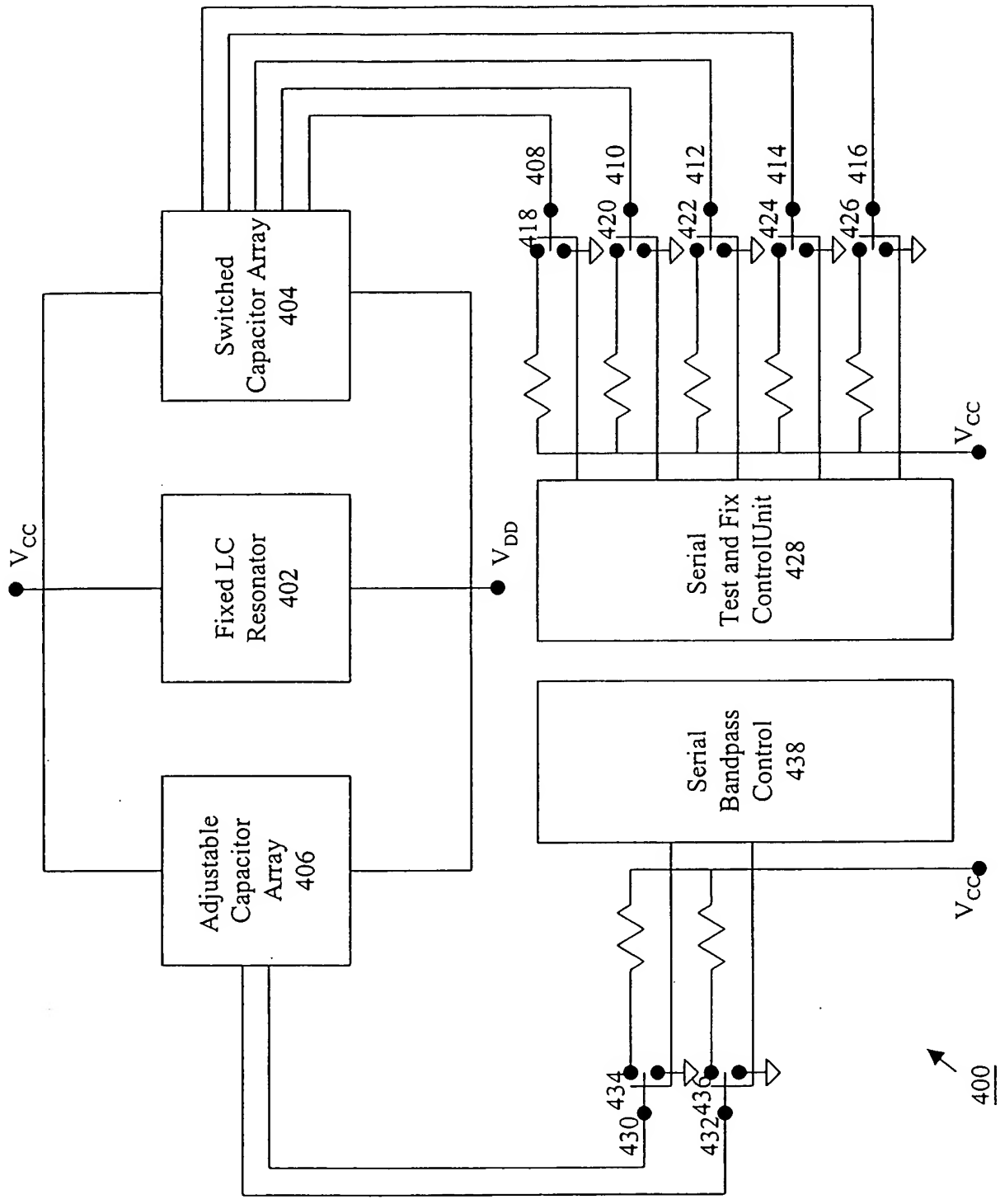
Figure 3


Switched Capacitor Array 404
Fixed LC Resonator 402
Adjustable Capacitor Array 406
Serial Test and Fix ControlUnit 428
Serial Bandpass Control 438
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V_{DD}
V_{CC}
V_{CC}
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410
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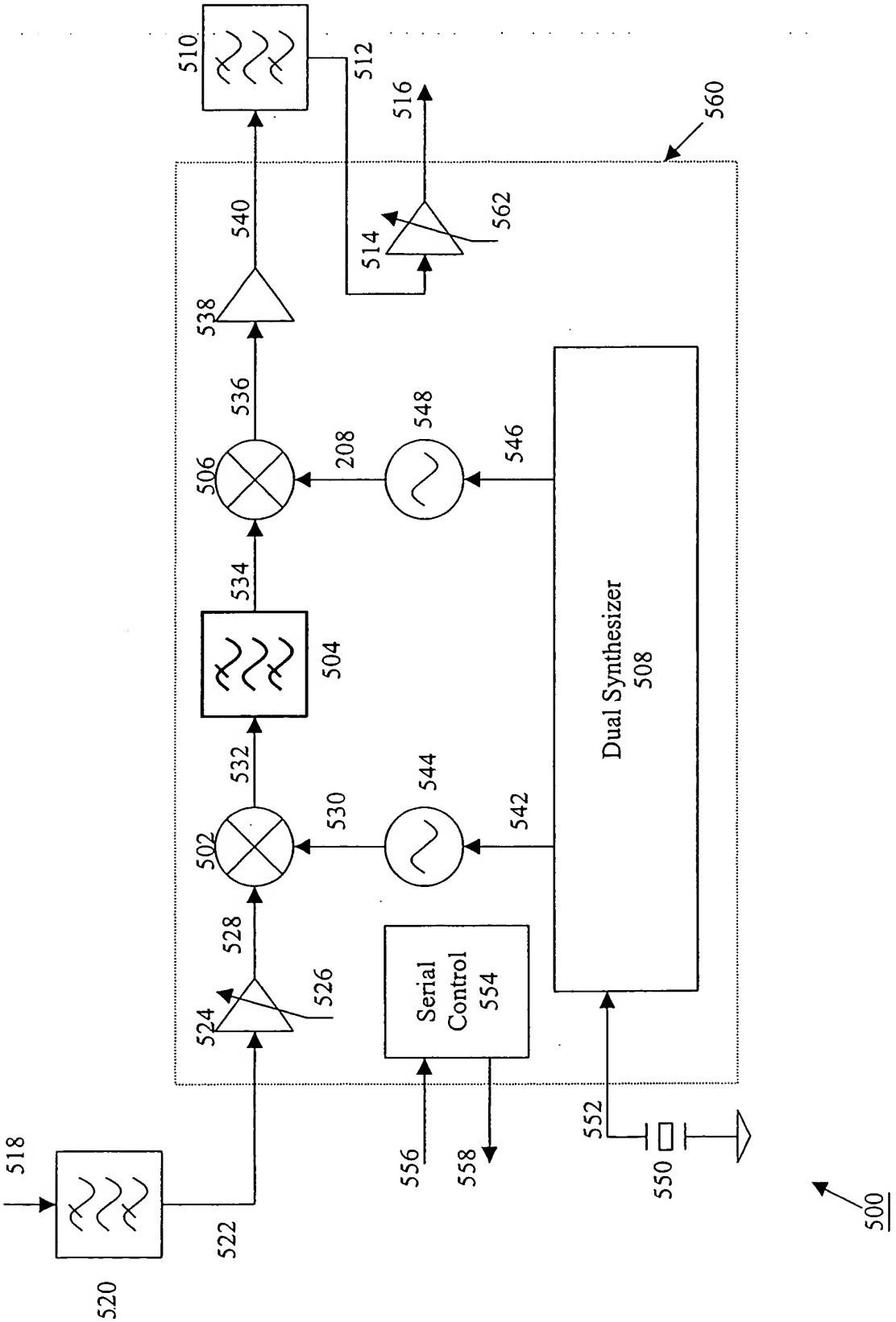
Figure 4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Serial
Control
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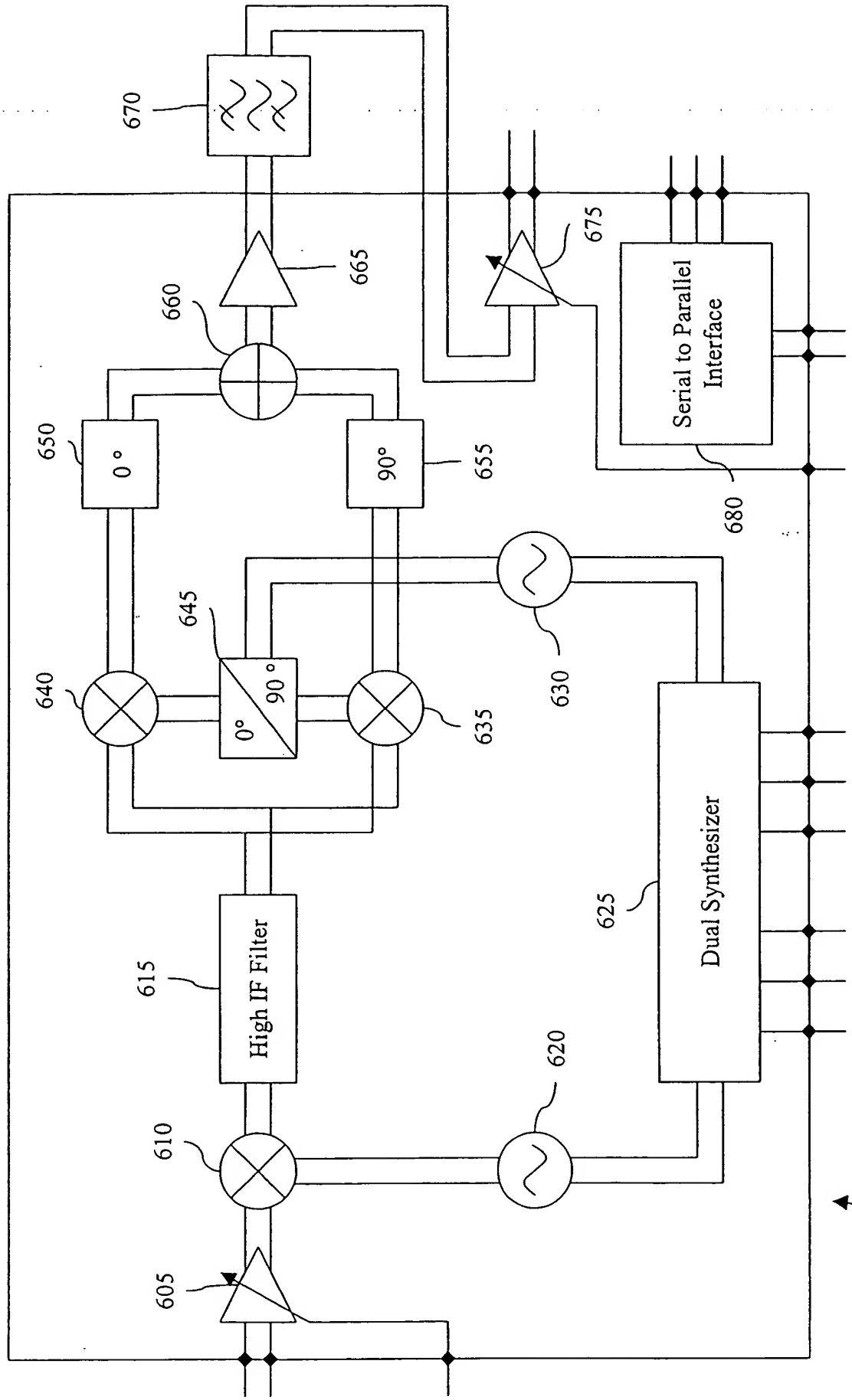
Figure 5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640
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90 °
635
630
625
Dual Synthesizer
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High IF Filter
620
610
605
600

Figure 6

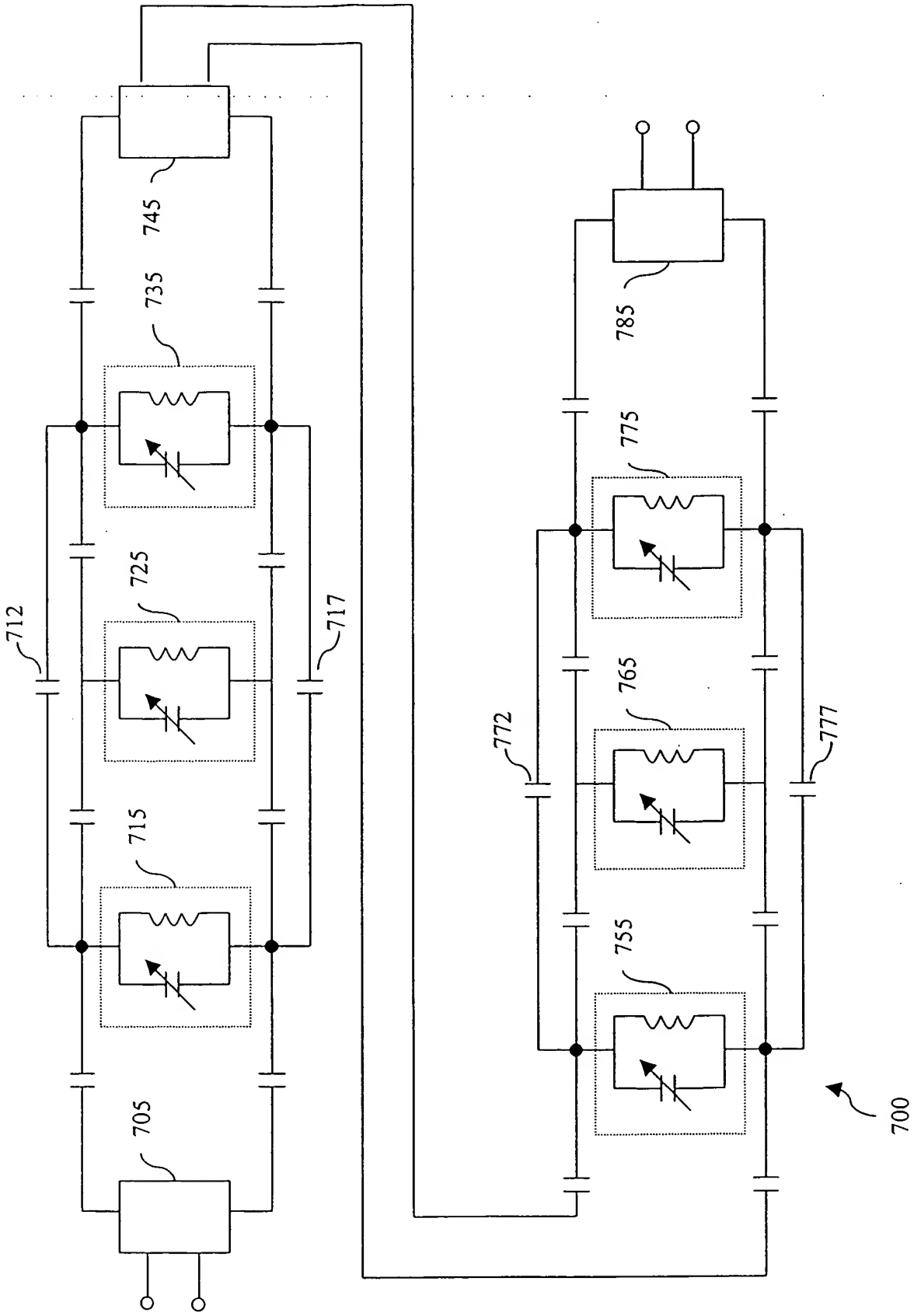

Figure 7

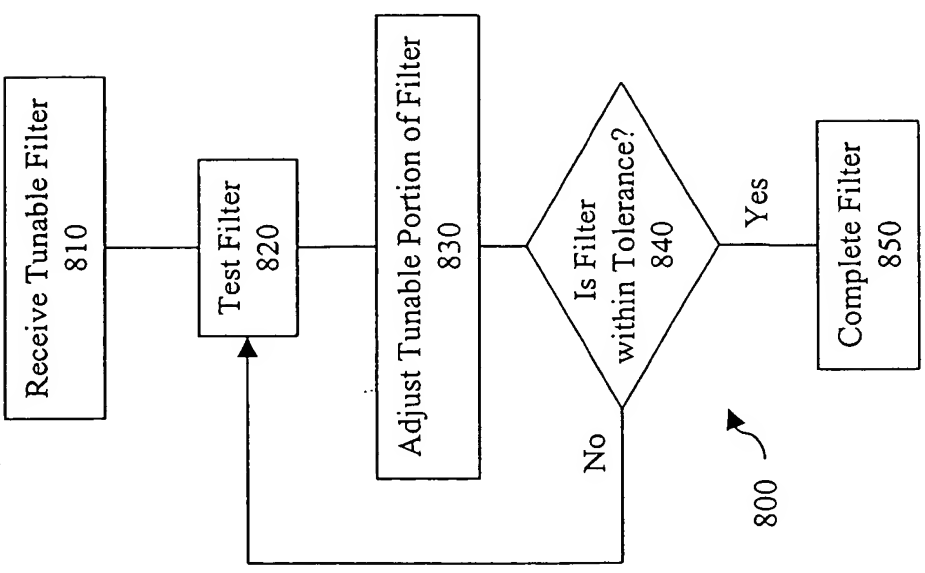

Figure 8

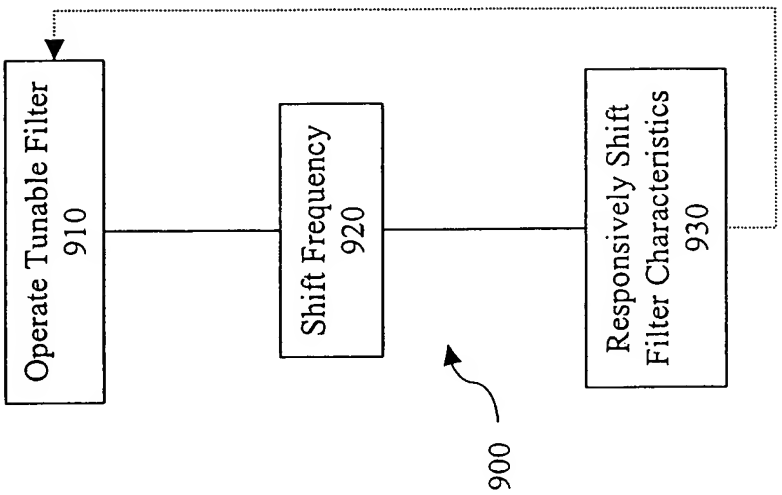

Figure 9